a data address generator coupled to the bus to address the memory on behalf of a requesting device.

a1 cont

3. (Amended) The system of claim 2, wherein the digital signal processor further comprises an arithmetic unit to perform arithmetic operations in the digital signal processor.

4. (Amended) The system of claim 3, wherein the arithmetic unit further comprises a branch metric unit to perform branch metric calculations.

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a2

6. (Amended) The system of claim 5, further comprising one or more registers in the arithmetic unit addressable by the data address generator.

7. (Amended) The system of claim 1, wherein the butterfly coprocessor further includes a plurality of butterfly units to perform butterfly operations.

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a3

9. (Amended) The system of claim 8, wherein the plurality of butterfly units in the butterfly coprocessor are coupled to further perform add-compare-select operations at the direction of the digital signal processor.

10. (Amended) The system of claim 8, wherein the plurality of butterfly units in the butterfly coprocessor are coupled to further perform approximations of logarithmic sum exponential operations at the direction of the digital signal processor.

11. (Amended) The system of claim 8, wherein the data address generator is coupled to access a path metric retrieved from a path metric memory.

a3 cont

12. (Amended) The system of claim 11, wherein the data address generator of the digital signal processor is coupled to retrieve a branch metric from the branch metric unit.

a4

17. (Amended) A method comprising:

receiving a request to decode a bit stream, wherein the bit stream was encoded by an encoder and the encoder is described using a trellis diagram;

identifying a stage of the trellis diagram;

computing branch metrics for all nodes of the stage;

retrieving path metrics for a different stage of the trellis diagram from a memory; and

simultaneously calculating new path metrics for each node of the stage.

18. (Amended) The method of claim 17, further comprising:

storing the new path metrics for each node of the stage in the memory; and

identifying a new stage of the trellis diagram.

a5

21. (Amended) A system comprising:

a digital signal processor, comprising:

a bus connectable to a memory;

a data address generator and

an arithmetic unit; and

a butterfly coprocessor coupled to the digital signal processor to perform an operation scheduled by the digital signal processor.